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Fully Reused VLSI Architecture of FM0/Manchester Encoding Technique for Memory Application

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ABSTRACT

In this paper a fully reused VLSI architecture of FM0/Manchester encoding technique for memory application has been proposed. In this paper we are encoding the 1 bit data into 16 bit data and storing it into a memory of certain address location given by the linear feedback shift register (LFSR),whose input is taken from the pseudo random sequence generator (PRSG). The encoded 16 bit data is stored into memory controller; the encoded data is decoded back into 1 bit data under the condition: when MSB bit is at logic state 1. By using FM0/Manchester encoding and decoding technique, the data will be secure , this process is easy and faster to carry out. This paper develops a fully reused VLSI architecture, and also exhibits an efficient performance.

Keywords: FM0/ Manchester encoder, Linear feedback shift register (LFSR), Pseudo random sequence generator (PRSG), Memory controller.

The FM0/Manchester encoding has many applications, such as Dedicated short Range communication, Digital signal processing, Memory applications etc. Firstly in DSRC application, the FM0/Manchester encoding using similarity oriented logic simplification (SOLS) technique was used. DSRC is a protocol for one or two way medium range communication. DSRC is categorised into two types

1. Automobile to Automobile.

2. Automobile to Roadside.

- In automobile to automobile, DSRC provides the means of sending the message and transmitting among the automobiles for safety issues public information announcement.
- In automobile to roadside, DSRC limelight's on the intelligent transportation service, such as electronic toll collection.

Here, in this paper we are using FM0/Manchester encoding technique for memory applications. Here the FM0 encoder , encodes the 1 bit data into 16 bit and stores in certain memory location given by LFSR. The encoded data is again decoded back into 1bit, by performing XOR operation of LFSR address bits and memory controller output bits. When we get the MSB bit as logic state 1, then the encoded data of 16 bit is decoded back into 1 bit.

The VLSI architecture of FM0 and Manchester encoders are analysed as follows.

REVIEW OF VLSI ARCHITECTURES FOR FM0 ENCODER AND MANCHESTER ENCODER

The literature [1] proposes a fully reused VLSI architecture of FM0/Manchester encoding using similarity oriented logic simplification (SOLS) technique for DSRC application; The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. In this paper, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. The literature [2] proposes a VLSI architecture of Manchester encoder for optical communications. This design adopts the CMOS inverter and the gated inverter as the switch to construct Manchester encoder. It is implemented by 0.35-μm CMOS technology and its operation frequency is 1 GHz. The literature [3] further replaces the architecture of switch in [2] by the nMOS device. It is realized in 90-nm CMOS technology, and the maximum operation frequency is as high as 5 GHz. The literature [4] develops a high-speed VLSI architecture almost fully reused with Manchester and Miller encodings for radio frequency identification (RFID) applications. This design is realized in 0.35-μm CMOS technology and the maximum operation frequency is 200 MHz. The literature [5] also proposes a Manchester encoding architecture for ultrahigh frequency (UHF) RFID tag emulator. This hardware architecture is conducted from the finite state machine (FSM) of Manchester code, and is realized into field-programmable gate array (FPGA) prototyping system. The maximum operation frequency of this design is about 256 MHz. The similar design methodology is further applied to individually construct FM0 and Miller encoders also for UHF RFID Tag emulator [6] . Its maximum operation frequency is about 192 MHz. Furthermore, [7] combines frequency shift keying (FSK) modulation and demodulation with Manchester codec in hardware realization.

CODING PRINCIPLES OF FM0 CODE AND MANCHESTER CODE

In the following discussion, the clock signal and the input data are abbreviated as CLK, and *X*, respectively. With the above parameters, the coding principles of FM0 and Manchester codes are discussed as follows.

A. FM0 ENCODING

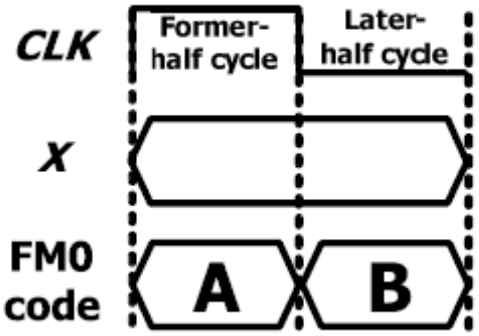

Figure 1. Code word structure of FM0

As shown in Fig. 1, for each *X*, the FM0 code consists of two parts: one for former-half cycle of CLK, *A*, and the other one for later-half cycle of CLK, *B*. The coding principle of FM0 is listed as the following three rules.

1) If *X* is the logic-0, the FM0 code must exhibit a transition between *A* and *B*.

2) If *X* is the logic-1, no transition is allowed between *A* and *B*.

3) The transition is allocated among each FM0 code no matter what the *X* is.

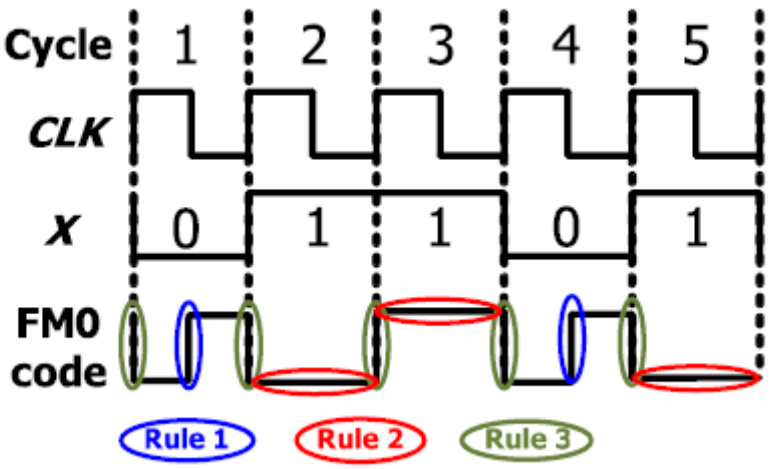

Figure 2. Illustration of FM0 coding example.

A FM0 coding example is shown in Fig. 2. At cycle 1, the *X* is logic-0; therefore, a transition occurs on its FM0 code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FM0 code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the *X* of logic-1.

Thus, the FM0 code of each cycle can be derived with these three rules mentioned earlier.

B. MANCHESTER ENCODING

The Manchester coding example is shown in Fig. 3. The Manchester code is derived from

$$X \oplus \text{CLK}. \qquad (1)$$

The Manchester encoding is realized with a XOR operation for CLK and *X*. The clock always has a transition within one cycle, and so does the Manchester code no matter what the *X* is.

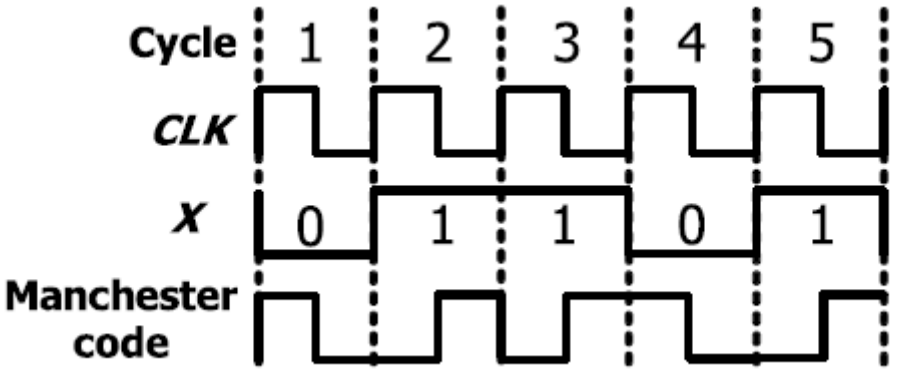

Figure 3. Illustration of Manchester coding example.

III. PROPOSED DESIGN

These articles are implemented using HDL designer for synthesis and Model Sim for simulation. To give an objective evaluation, the proposed VLSI architecture is realized with HDL design-flows.

PROPOSED BLOCK DIAGRAM

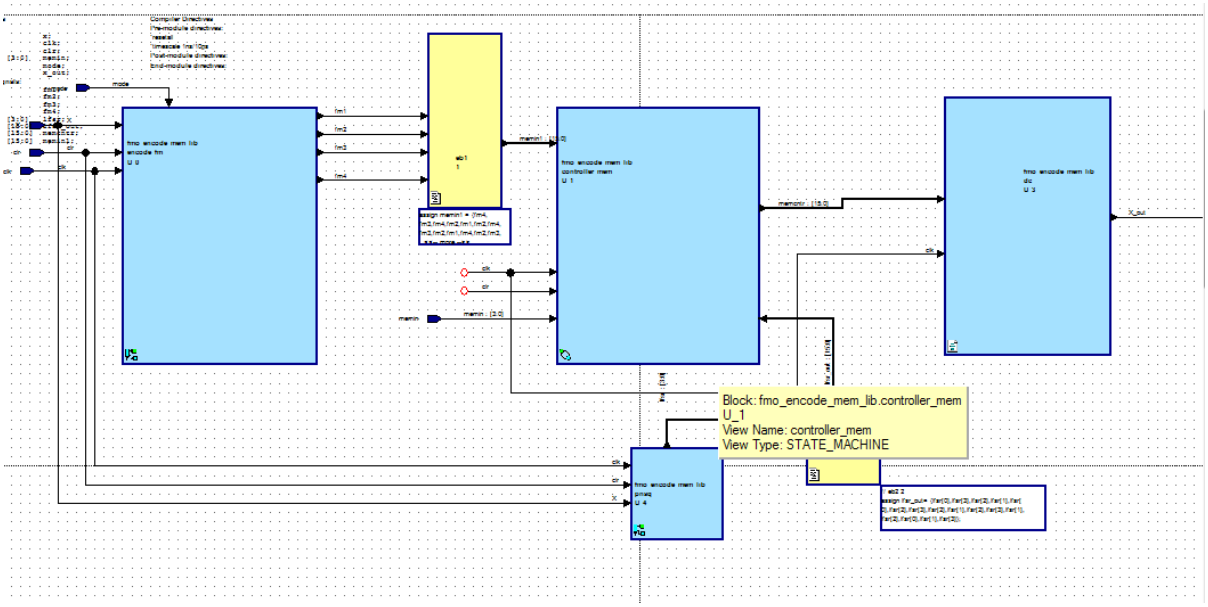

Fig 4. Block diagram

The above block diagram consists of 5 main blocks.

1. Encoding block.
2. Pseudo random sequence generator (PRSG).
3. Linear feedback shift register (LFSR) .
4. Memory controller block.
5. Decoding block.

FUNCTIONS OF THESE BLOCKS

Encoding block : Here in this block it consists of 4 modules of FM0 encoder, X bit is the input given to al the 4 modules. Inputs to this block are X bit,clk, clr, and mode.

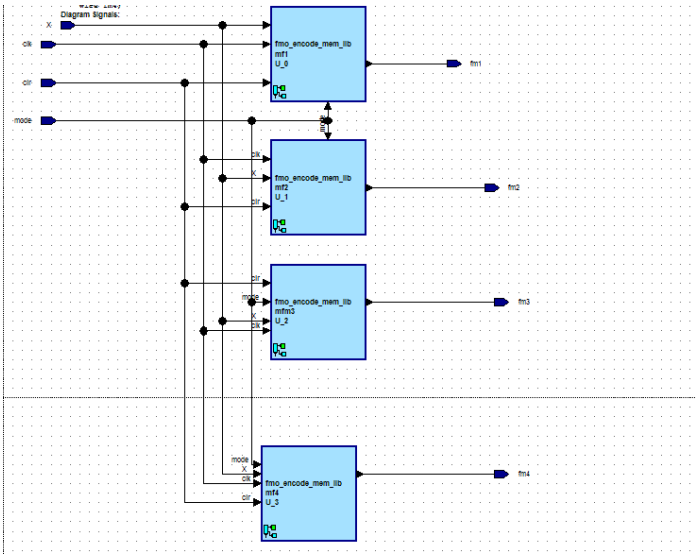

Fig 5. FM0 encoder modules

Here the 1 bit input data is encoded into the 16 bit data and sent to the memory controller block.

1. Pseudo Random Sequence Generator: It is an algorithm for generating a sequence of numbers whose properties approximate the properties of sequences of random number. Here it generates sum random 4 bit numbers and sends it to linear feedback shift register (LFSR).

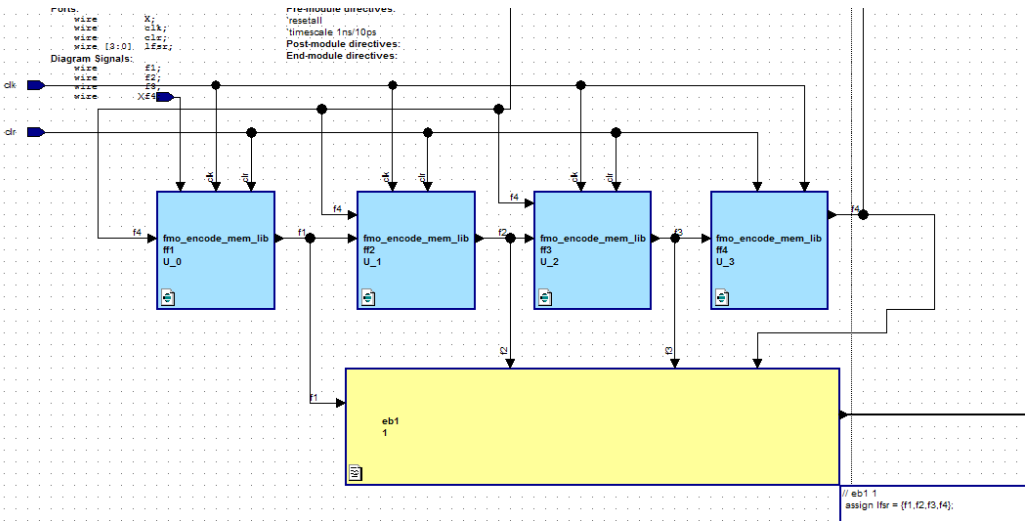

Fig 6. Block diagram of PRSG

1. Linear Feedback Shift Register (LFSR) : LFSR gives the address location where the 16 bit encoded data has to be stored in memory controller. The PRSG sends the 4 bit input i.e. nothing but the address location to the LFSR, where encoded data has to be stored.
2. Memory Controller : In memory controller , firstly the 4 bit encoded data from 4 modules of FM0 encoder are concatenated into 16 bit encoded data. This 16 bit encoded data is stored into a particular address location sent by LFSR.
3. Decoding block: Now the 16 bit encoded data stored in memory is XOR with the address location of LFSR. If the MSB bit of the XOR output is at logic 1 , then in only that condition the data will be decoded back into 1 bit, Because that is the condition we have designed for.

EXPERIMENTAL RESULTS

Here the block diagram shown in the fig 4 is simulated using Model sim and by giving the following data as input

X= 1, Clock = clock, Clear=1, Mode = 1, Memory input= 1010

We obtain the following results shown in below figures.

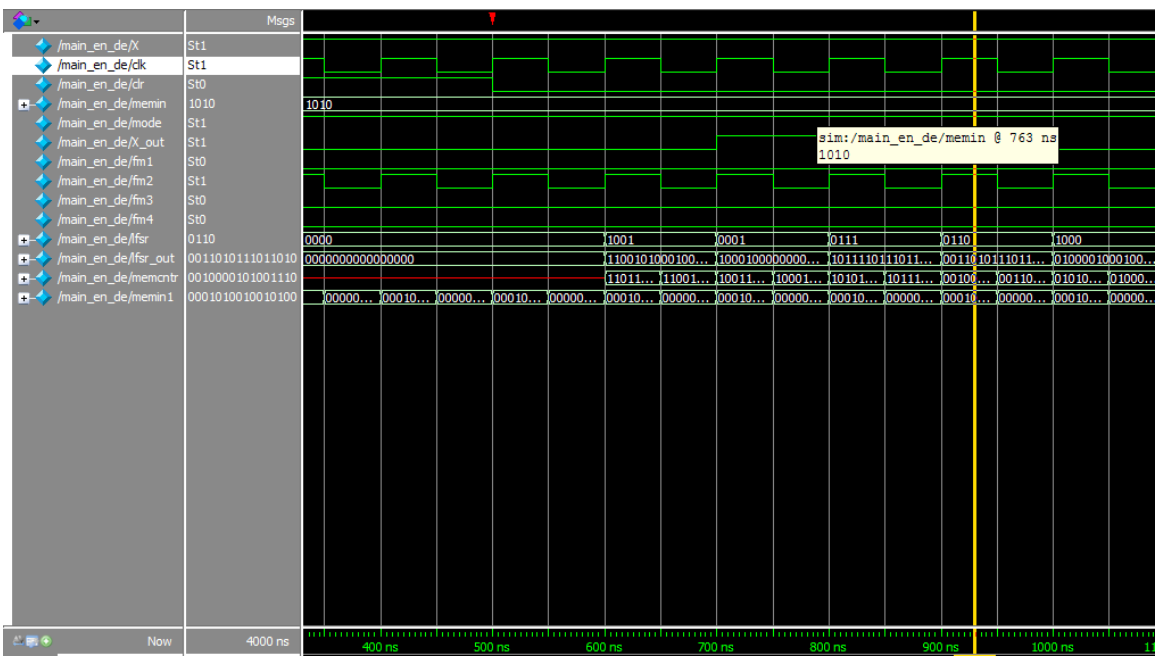

Fig 7. Experimental Results 1

Here from the above figure 7, by analysing the data

LFSR out = 0011010111011010 and

Memory input= 0001010010010100.

Now by performing the XOR operation we get the output of Memory controller = 0010000101001110. As the MSB bit of this 16 bit data is 0, the encoded data is not decoded.

Here from the below fig 8, by analysing the data

LFSR out=1011110111011110 and

Memory input= 0000000000000000.

Now by performing the XOR operation we get the output of memory controller= 1011110111011110. As here the MSB bit of this 16 bit encoded data is "1" the encoded data is decoded back into 1 bit.

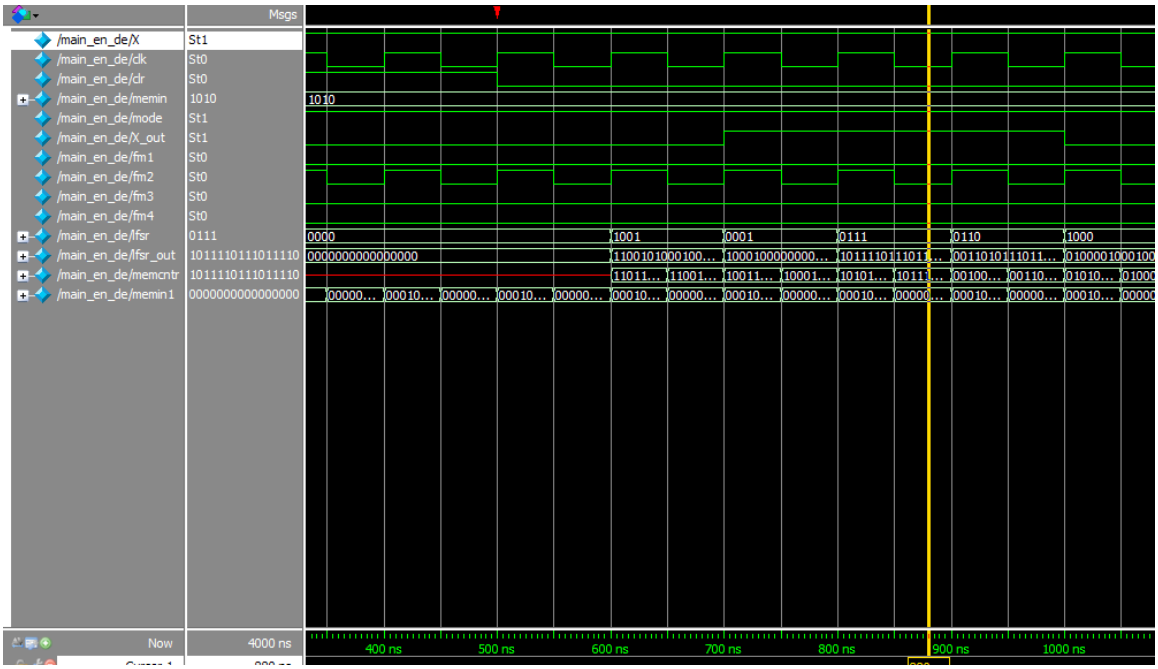

Figure 8. Experimental Results 2

CONCLUSION

The fully reused VLSI Architecture of FM0/Manchester encoder for memory applications is effective and powerful in securing the data, as compared to the other encoding techniques. FM0/Manchester encoder are easy to perform operations and faster.Hence these encoding techniques are efficient.